I. Introduction

LNA is one of the important components in the receiver path. Its noise figure dominates the overall system. Hence, low noise figure and sufficient gain are critical LNA performance parameters. Besides, low power consumption is also essential for commercial applications. Recently, efforts attempting to design mm-wave amplifiers by using CMOS processes have been reported[1],[2],[3]. using 0.13 μm and 90 nm CMOS. In this paper, the aim of this work is to design a V-band low-noise amplifier that is suitable for SoC and wireless communication systems. It achieves a peak gain of 11.7 dB while consuming 21.6 mW.

II. LNA Circuit Design

This circuit was fabricated in commercial standard 0.13 μm 1P8M CMOS process. Passive elements including metal-insulator-metal (MIM) capacitors are available between metal 7 and metal 8. The schematic of the three-stage cascaded common source V-band LNA is shown in Fig. 1. The noise factor (F) of common source amplifier is usually defined as:

\[ F = 1 + \frac{R_i}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha Q_{in}} \left( \frac{\omega_b}{\omega_T} \right) \]  

From (1), the noise factor is proportional to \( \omega_b \), and inversely proportional to \( Q_{in} \) as well as \( \omega_T \). The \( f_T \) of CMOS 0.13 μm NMOS transistor is around 91 GHz [2]. In order to obtain a lower noise figure, the common source structure is adopted. In addition, the sizes of the transistors are chosen under the consideration of low power consumption while maintaining a desire circuit performance. First stage of the LNA is based on noise figure consideration. The optimal width for lower noise input stage is 18 fingers with a total gate width of 36 μm corresponding a current density of 167 μA/μm at a supply voltage of 1.2 V and gate bias of 0.8 V.

In this work, thin-film microstrip (TFMS) line is used for the matching networks and all interconnections. The TFMS consists of the top metal layer (M8) as the signal microstrip lines, and the first metal layer (M1) as the ground plane. Compared to coplanar waveguide (CPW), microstrip lines are more flexible in interconnection. As CMOS technologies advanced beyond the 0.18 μm node, increasingly stringent metal density rules prohibited the design of solid ground planes. In order to accommodate these restrictions, metal ground planes must now be slotted [4]. Fig. 2 shows the simulated effective permittivity of the TFMS agrees with Mangan’s work [4] under the same conditions. Thus, the reasonable effective permittivity applied to this work is chosen to 3.6.

The L-section input matching network (IMN) is widely used for LNA design, as shown in Fig. 1. The IMN consists of a 50 Ω transmission line (L1) and a short-terminated (through capacitance \( C_{bypass} \)) stub (L2) to perform the matching to 50 Ω. Similarly, the output matching
network (OMN) is accomplished by the same method. Besides, all interconnections and G-S-G RF pads included in this design were simulated by EM simulation tool as well as Agilent ADS.

III. Measurement Technique and Results

In the two-tone test, in order to generate a two-tone signal, a V-band magic tee is acted as a power combiner. And all losses from the adaptors and cables were de-embedded in experimental results. However, the two-tone test was measured at 51 GHz because of the limitation of signal source in our lab, but the result is still meaningful. In the measurement of noise figure, the cable losses, probe losses and DUT intrinsic noise are measured by NFA. According to the Friis’ formula, we can define $F_{\text{measured}}$ as:

$$F_{\text{measured}} = F_1 + \frac{F_{LNA} \cdot (1 - G_1)}{G_1 G_{LNA}} + \frac{F_3}{G_1 G_{LNA}}$$

Where, $F_1$ is the noise factor of the input cable and input G-S-G probe. Similarly, $F_3$ is the noise factor of the output cable and output G-S-G probe. From (2), assumed that $G_{LNA}$ is sufficient enough, the $F_{LNA}$ is re-expressed as:

$$F_{LNA} = G_1 \left( F_{\text{measured}} \right) \Rightarrow NF_{LNA} = NF_{\text{measured}} - NF_1$$

According to (3), if we know the loss of the 1st stage, the additional noise can be calibrated out. Fig. 3(left) is the calibration of the NFA together with the V-band noise source, amplifier and down-converter. The V-band noise figure measurement system is shown in Fig. 3(right).

The LNA was measured on-wafer using high frequency probes. The $V_{DD}$ supply voltage and gate bias voltage were 1.2 V and 0.8 V respectively. Since the parasitic effects of the RF pads were incorporated while performing simulation, no de-embedding was required on the measured results. The measured input and output return loss is plotted in Fig. 4. The input and output return losses close to -9.4 dB and -16 dB respectively. Fig. 5 shows the small signal gain is 11.7 dB at 50 GHz with a noise figure of 7.9 dB, while consuming 21.6 mW from a 1.2-V supply. A 3-dB bandwidth is 6 GHz. As shown in Fig. 6, the measured input 1-dB compression point ($P_{1\text{dB}}$) is -9.5 dBm and IIP3 is -1.65 dBm at 51 GHz. Fig. 7 is the spectrum of the two-tone test with a 20-MHz tone spacing. The LNA chip micrograph is shown in Fig. 8, and the chip size is $1.39 \times 0.76 \text{ mm}^2$. Table I shows the performance comparison of the V-band CMOS LNA with reported works. The designed LNA demonstrates a low power consumption and more than 10-dB gain.

IV. Conclusions

This paper presented the design, fabrication, and measurement of proposed V-band LNA. It was fabricated in a TSMC 0.13-μm standard CMOS process. Compared to the other works using 0.13 μm CMOS, this work has shown that the V-band LNA reduced power consumption successfully. This circuit is measured via on-wafer probing. The V-band LNA has demonstrated a gain of 11.7 dB, a minimum noise figure of 7.9 dB. The input $P_{1\text{dB}}$ is -9.5 dBm and IIP3 is -1.65 dBm at 51 GHz. The total power consumption is 21.6 mW from a 1.2 V power supply.

V. References


### VI. Figures

**Fig.1.** Circuit schematic of a V-band LNA.  
**Fig.2.** Effective permittivity.

**Fig.3.** Calibration and measurement of noise figure set-up.

**Fig.4.** Measured $S_{11}$ and $S_{22}$.  
**Fig.5.** Measured $S_{21}$ and NF.
VII. Table

Table 1. Performance comparison of the V-Band CMOS LNA with reported works

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech. (CMOS)</th>
<th>Supply Voltage (V)</th>
<th>Peak Gain Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>IIP3 (dBm)</th>
<th>Power Consumption (mW)</th>
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<tr>
<td>[1]</td>
<td>0.13 μm</td>
<td>1.5</td>
<td>57</td>
<td>12</td>
<td>8.8</td>
<td>-</td>
<td>54</td>
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<td>24.7</td>
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<td>1</td>
<td>79</td>
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<td>[3]</td>
<td>90 nm</td>
<td>1.5</td>
<td>58</td>
<td>14.6</td>
<td>4.5 (sim.)</td>
<td>-6.8</td>
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<td>[5]</td>
<td>0.13 μm</td>
<td>1.4</td>
<td>60</td>
<td>3.8</td>
<td>6.4 (sim.)</td>
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<td>18.5</td>
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<tr>
<td>[6]</td>
<td>90 nm</td>
<td>1.7</td>
<td>60</td>
<td>5.1</td>
<td>7</td>
<td>-1.9</td>
<td>18.5</td>
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<tr>
<td>This Work</td>
<td>0.13 μm</td>
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<td>50</td>
<td>11.7</td>
<td>7.9</td>
<td>-1.65</td>
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