A 6-10-GHz CMOS Power Amplifier with an Inter-stage Wideband Impedance Transformer For UWB Transmitters

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Abstract — A 6-10-GHz broadband CMOS power amplifier (PA) for Ultra-wideband (UWB) transmitters is presented. An inter-stage wideband impedance transformer is designed between the small-signal stage and driver amplifier for the wideband operation. The UWB PA is implemented in the 0.18-μm 1P6M standard UMC CMOS process. Fully on-wafer measurement shows that the fabricated PA exhibits an average small-signal gain, P1dB, and PAE of 8.5 dB, 5 dBm, and 14.4%, respectively, from 6 to 10 GHz. A low power consumption of only 18 mW is obtained from a voltage of 1.5 V.

I. INTRODUCTION

Ever since the Federal Communications Commission (FCC) released the spectrum allocated from 3.1 to 10.6 GHz for the UWB technology, abundance of research has been devoted for its wide-range application. UWB is proposed to transmit a very fast data rate and a very low radiated power constrained to the level of -41.3 dBm/MHz [1].

Since the radiated power is constrained below -5.5 dBm at 6-10 GHz due to the Effective Isotropic Radiated Power (EIRP) limit regulated by FCC, much attention does not need to be focused on the output power but the bandwidth, linearity and power consumption. Such a broadband requirement on the transmitting PA which is the most power-consumed circuit, imposes numerous difficulties for achieving a low power consumption and enough output power. The UWB PAs cover the frequency band of 3.1-4.8 GHz and 3.1-10.6 GHz have been widely implemented in the CMOS technology [2]-[5].

The power consumptions among these fabricated UWB PAs ranged from 25 to 84 mW. To alleviate the consumed power on the transmitter design, the power consumption of the designed UWB PA should be reduced.

In this paper, the design of a fully integrated 6-10-GHz CMOS PA adopts two-stage topology, the first stage is the small-signal amplifier dominates the small-signal gain and the last stage is the driver amplifier drives the necessary output power. An inter-stage wideband impedance transformer is designed between these two stages and provides an enough high wideband impedance (about 240 Ω) to lower the power consumption of the first stage. The driver amplifier operates in the class-AB region for the required output power and the demand of low-power consumption.

II. DESIGN APPROACH

A. Stage-1 small-signal amplifier

As shown in Fig. 1, the common-gate transistor $M_1$ can achieve a good impedance matching by appropriately setting its transconductance of 20 mS. Based on the postulation that input matching is good over 6 to 10 GHz, the equivalent transconductance $G_{m,eq}$ of stage 1 can be derived as

$$G_{m,eq} = \frac{1}{2} \cdot \frac{g_{m2}}{g_{m2} + jω(C_{gds1} + C_{p2})} \cdot g_{m1} \quad (1)$$

$G_{m,eq}$ may be slightly degraded by $C_{gds1}$ and $C_{p2}$ in higher frequencies and will be about 10 mS under the good input matching. Another common-gate transistor $M_2$ is stacked on $M_1$ for a good isolation. To have a minor effect on the inter-stage network, a large inductor $L_C$ is used for directly biasing the small-signal amplifier with $V_{DD}$. 

Section II describes the design approach of the small-signal amplifier, driver amplifier and wideband impedance transformer. Section III represents a detailed examination on the small-signal voltage gain and output power. The PA is implemented in a 0.18-μm 1P6M UMC CMOS process.
Since the maximum output-power limit is around -5.5 dBm at the 6-10-GHz UWB band, for more linear operation of the designed PA the back-off option on the output power is adopted here. If the output network is assumed to be lossless, then the output power of the driver amplifier can be expressed as

\[ P_{\text{drive}} = \frac{v_{o,p-p} \times i_{o,p-p}}{8} \]  

(2)

For this PA design, if \( P_{\text{Driver}} = 5 \text{ dBm} (= 3.2 \text{ mW}) \), \( v_{o,p-p} = 2.7 \text{ V} \) and a class-AB design, the calculated DC current is about 4.7 mA for the linear operation. As shown in Fig. 2 (a), the conventional PA has to achieve a simultaneous maximum voltage and current swing for the maximum output power. For the UWB PA, a maximum voltage swing and only smaller current swing will be able to satisfy the output power demand in UWB transmitters. Hence, the load for the designed PA will be much larger than that of the conventional PA [6].

### C. Principle of the impedance transformer

Fig. 2(b) shows a prototype of the wideband impedance transformer. At first, when without the resistance \( R_s \), the series and shunt reactance can be derived as

\[ X_{\text{series}} = \left(\frac{f}{f_{f1}}\right)^2 - 1 \]

\[ X_{\text{shunt}} = \frac{\omega C_1}{1 - \left(\frac{f}{f_{f1}}\right)^2} \]  

(3)

where \( f/2\pi \sqrt{L_1 C_1} = f_{f1} \approx f_{f2} = 1/2\pi \sqrt{L_2 C_2} \) are chosen at around the middle frequency. From Eq. (3), \( C_2 \) and \( L_1 \) control the series and shunt reactance when off the central frequency. From Eq. (3) it is observed that, for frequencies below the central frequency, \( X_{\text{series}} \) exhibits as a series capacitance and \( X_{\text{shunt}} \) as a shunt inductance, respectively, and vice versa for that above the central frequency. Therefore, the combined reactance of the two branches can be mitigated due to the opposite property of reactances. However, the large reactance caused by the shunt branch around the central frequency will let the combined reactance change abruptly.

To tackle this problem, a selectable resistance \( R_s \) is inserted in series with \( L_1 \) to reduce the large reactance around 8 GHz until an acceptable level. The equivalent resistance and reactance of the shunt branch after the added \( R_s \) can be expressed as

\[ R_{\text{shunt}} = \frac{R_s}{1 - \left(\frac{f}{f_{f1}}\right)^2} \]

\[ X_{\text{shunt}} = \frac{\omega R_s C_1}{1 - \left(\frac{f}{f_{f1}}\right)^2} \]  

(4)

From Eq. (5), the resistance and reactance are altered to values determined by the passive components of \( R_s, L_1 \) and \( C_1 \). As shown in Fig. 3, with the addition of \( R_s \), the normalized resistances and reactances are lowered greatly around the frequencies offset 1 GHz from the central frequency. Finally, few varied resistances and reactances of the shunt branch, over 6-10-GHz frequency band, benefit the broadband performance as it being a load for wideband amplifiers.

As shown in Fig. 4, the resistance, reactance and impedance of the combined network (combined the series and shunt branches with the addition of \( R_s \)) with \( L_c \) and \( C_x \) are few altered over the 6-10-GHz frequency band. The resulted normalized impedance is fluctuated only ±34 Ω in the desired frequency band and the gradually grown attitude of it, from 8 GHz to 10 GHz, prevents the degradation of \( G_{\text{in,eq}} \) in Eq. (1).

As shown in Fig. 1 and Fig. 5, the combined network is inserted between stage 1 and stage 2 for the wideband gain produced by stage 1. The selection of RF choke \( L_c \) should be large enough to cause a minor effect on the inter-stage network. \( C_5 \) can be substituted major by \( C_{g32} \) and \( C_4 \) is replaced by the merged capacitance of \( C_{g31} \) and \( (1+G_{22}) C_{p31} \) from stage 2. \( G_{22} \) is the voltage gain of stage 2 and the second term is the miller capacitance. As described in part A., due to the 10 mS-\( G_{\text{in,eq}} \), a 7.6-dB small-signal gain of stage 1 can be achieved as an average \( |Z_{\text{combined}}| \) of about 240 Ω (Fig. 4).

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**Fig. 2** (a) Load-line representation of PAs and (b) prototype of the wideband impedance transformer.

Around the central frequency, Eq. (4) is simplified as Eq. (5).

\[ R_{\text{shunt}} = \frac{L_1}{C_1} \quad X_{\text{shunt}} = -\frac{R_s C_1}{\omega} \]  

(5)
III. SMALL-SIGNAL GAIN AND OUTPUT POWER

Based on the assumption of a good input and output matching, the small-signal voltage gain of the overall circuit shown in Fig. 1 can be expressed as Eq. (6). $X_1$ and $X_2$ are the equivalent series reactance of the shunt and series branch, respectively. The first to the last term is the gain of the stage 1, inter-stage transformer, stage 2 and output matching network, respectively. The first and the third term provide gains while the last term introduces a degradation of around 7 dB, thus the combined topology of stage 2 and the output matching network induces a much minor gain compared to stage 1. Since $X_1$ and $X_2$ are partially cancelled out each other from 6 to 10 GHz, the second term is around a 0-dB contribution. The output peak-to-peak voltage swing of stage 1 is 1V, therefore the output (complex) power is about -2.5 dBm. Finally, the output power driven by stage 2 is about 5 dBm.

IV. EXPERIMENTAL RESULTS

The designed UWB PA has been fabricated in the 0.18-μm UMC CMOS process. The die micrograph of this PA is shown in Fig. 6 and its size is 0.82 × 1.32 mm². The measurement is implemented on wafer. Fig. 7 shows the measured input return loss larger than 7 dB from 6 to 9.8 GHz and the average gain of 8.5 dB from 6 to 10 GHz. The measured OIP3 and PAE are shown in Fig. 8. The measured OIP3 is almost 5 dBm from 6 to 9.8 GHz except for 9.8 to 10 GHz and PAE ranged from 11.4 % to 17.6 % at 6-9.8 GHz and drops until 8.8 % at 10 GHz. The designed power amplifier consumes 18 mW from a 1.5-V DC voltage. The measured performance of this power amplifier is summarized and compared with [2]-[4] in Table I.

V. CONCLUSION

A 6-10 GHz UWB PA, fabricated in the 0.18-μm UMC CMOS process, incorporated the inter-stage wideband impedance transformer is presented. A broadband gain implies the almost-constant input impedance presented by the inter-stage transformer. The average maximum output power, at the 6-10-GHz frequency band, impelled by the designed power amplifier is 5 dBm which is 10.5 dB higher than the maximum than the maximum output power regulated by FCC at UWB high-band frequency. The measured output power suggests that this power amplifier would operate more linear in actual UWB transmitters while consuming just a low power of 18 mW from a 1.5-V DC voltage.

REFERENCES


Fig. 3 Normalized resistance and reactance of the shunt branch with and without $R_1$ of 55 Ω.

Fig. 4 Normalized resistance, reactance and impedance of the combined network with and without $L_c$ and $C_x$.

Fig. 5 Simplified topology of the designed power amplifier.
TABLE I

SUMMARY AND COMPARISON OF UWB-PA PERFORMANCES

<table>
<thead>
<tr>
<th>Reference (Measurement)</th>
<th>CMOS Tech. (μm)</th>
<th>Freq. Range (GHz)</th>
<th>Avg. Gain (dB)</th>
<th>Avg. OP_{1dB} (dBM)</th>
<th>Power Consumption (mW)</th>
<th>Avg. PAE (%) (@ OP_{1dB})</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>0.18</td>
<td>6-10</td>
<td>8.5</td>
<td>5 @ 6-10 GHz</td>
<td>18 @ 1.5 V</td>
<td>14.4 @ 6-10 GHz</td>
</tr>
<tr>
<td>[2]</td>
<td>0.18</td>
<td>3.1-4.8</td>
<td>19</td>
<td>-4.2 @ only 4 GHz</td>
<td>25 @ 1.8 V</td>
<td>1.5 * @ only 4 GHz</td>
</tr>
<tr>
<td>[3]</td>
<td>0.18</td>
<td>3.1-10.6</td>
<td>-9</td>
<td>0 @ 3.1-10.6 GHz</td>
<td>25.2 @ 1.8 V</td>
<td>3.3 * @ 3.1-10.6 GHz</td>
</tr>
<tr>
<td>[4]</td>
<td>0.18</td>
<td>3-10</td>
<td>~11 *</td>
<td>8 * @ 3-10 GHz</td>
<td>84 @ 2 V</td>
<td>6.8 * @ 3-10 GHz</td>
</tr>
</tbody>
</table>

* Estimated values

\[
G_{Y_F} \approx \frac{1}{2} \left( \frac{S_{m2}}{S_{m2} + j\omega(C_{g1m} + C_{g2m})} \right) \left| g_{m1} |Z_{combined}| \right| \left| \frac{R_p + jX_1}{R_p + j(X_1 + X_2)} \right| \left| \frac{g_{m3} + j\omega C_{gd3}}{\frac{g_{md} + j\omega C_{gd1}}{2}} \right|
\]  

(6)

**Fig. 6** Die micrograph (0.82 × 1.32 mm²)

**Fig. 7** Measured input and output return loss and gain.

**Fig. 8** Measured OP_{1dB} and PAE.